UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,672	07/12/2001	Michimasa Funabashi	843.37558VX2	3073

20457 7590 06/04/2003

ANTONELLI TERRY STOUT AND KRAUS
SUITE 1800
1300 NORTH SEVENTEENTH STREET
ARLINGTON, VA 22209

EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/902,672	FUNABASHI, MICHIMASA	
	Examiner	Art Unit	
	Lex Malsawma	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/392,568* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 16, 2003 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 17-21, 23-26, and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmi et al. (5,990,060, hereinafter, "Ohmi") in view of Wang (6,087,243) and Okutani (5,135,608).

Regarding Claims 17-20, 23, and 25:

Ohmi discloses the following:

a processing solution containing hydrogen peroxide, hydracid fluoride salt (e.g., tetraalkyl ammonium fluoride), and water (note TABLE 1, in col. 9);

the processing solution includes HF and HF_2^- as etching seeds of silicon oxide (note col. 2, lines 32-34);

the processing solution can be utilized with ultrasonic vibration during the cleaning of a silicon wafer (note col. 3, line 67 to col. 4, line 44);

the processing solution can be utilized for cleaning the silicon wafer at a temperature as low as 40 °C (note col. 5, lines 7-16);

the processing solution is used to remove foreign materials deposited on a substrate after photoresist for ion injection or reactive ion etching is removed (note col. 2, lines 7-13), wherein a manufacturing process, including a cleaning process which utilizes the processing solution, is preferably performed with an apparatus comprising a plasma processing device (for photoresist removal) directly connected (or provided adjacent) to an ion injection device (or a reactive ion etching device), while a cleaning device is directly (or provided adjacent) to the plasma processing device (note col. 5, lines 41-62); and

a method of utilizing the processing solution comprising:

(a) providing a silicon wafer 3 covered with an insulating film **4** whose main surface is mainly formed of silicon oxide 4 (note Figs. 3), wherein the surface contains foreign material 6 from a previous step of removing a photoresist (note Fig. 5); and

(b) cleaning the surface of said silicon wafer with said processing solution ***covered by said insulating film 4 whose main surface is mainly formed of silicon dioxide*** such that the foreign material 6 is removed from the mainly silicon oxide surface (Fig. 6).

Ohmi **lacks** the following:

(1) specifying a sheet-by-sheet cleaning process;

(2) the device manufacturing process step (c) of removing the insulating film after the step (b) of cleaning to expose the surface to the silicon wafer; and

(3) the device manufacturing process step (d) of subjecting the silicon wafer to a heat-treatment after step (c) thereby to form a gate oxide film over the silicon wafer.

In regards to lacked-limitation (1), it is noted Ohmi discloses it is preferable to utilize a multi-module apparatus when implementing the cleaning process (note col. 5, lines 51-62). Okutani **teaches** a multi-module apparatus would have been available, wherein the multi-module apparatus has the ideal features necessary for implementing Ohmi's cleaning process into a semiconductor device manufacturing method. Okutani discloses (note abstract and Fig. 1) the apparatus allows dry processing and wet processing to be continuously effected without exposing the wafer to air (i.e., a contaminating atmosphere outside of the apparatus) wherein a substrate can be processed in a sheet-by-sheet manner. Therefore, lacked-limitation (1) is not considered to have patentable weight because an apparatus for sheet-by-sheet processing would have been commercially available at the time the current invention was made.

In regards to lacked-limitations (2) and (3), it important to note that Ohmi does not disclose, or is not specifically concerned with disclosing, process steps for forming any particular device, but rather, Ohmi discloses only process steps (or conditions) necessary to clean a substrate utilizing the processing solution. In other words, Ohmi discloses an important aspect of the current invention, i.e., a processing solution which contains hydrogen peroxide, hydracid fluoride salt, and water; and Ohmi discloses only pertinent steps for utilizing the processing solution in a cleaning process, wherein the cleaning process would be just one process out of a plurality of processes that would be required during a semiconductor device fabrication, for

example, other processes such as an ion-implantation process, a metallization process, a via forming process, etc. would also be necessary in a semiconductor device fabrication. Wang is cited to show processes that would typically be included in a semiconductor device fabrication. Wang **teaches** (in col. 2, lines 12-41) a pad oxide layer (i.e., a sacrificial oxide layer) is first formed on a surface of a substrate; various process steps are then performed, including an ion implantation step to form a retrograde well (note col. 2, lines 30-31); then remaining portions of the pad/sacrificial oxide layer is then removed (col. 2, lines 36-37); and after removal of said remaining portions, a gate oxide film is grown over the silicon wafer, wherein the gate oxide would most probably be thermally grown (note col. 2, lines 38-40) as is common in the art. The following important note is necessary at this point:

> In regards to Wang's disclosure of performing an ion implantation step (to form a retrograde well) prior to removing the remaining pad/sacrificial oxide, one of ordinary skill in the art would have realized that the ion implantation step would be performed by utilizing a resist pattern which is later removed, even though Wang does not specifically disclose the steps for the ion-implantation process. For example, note Ohmi's disclosure in col. 5 (lines 41-50), "[r]esist is always required from the photolithographic process to the next ion implantation process...". One of ordinary skill in the art would realize that numerous resist patterning and removal steps are generally required during device fabrication, wherein according to Ohmi's disclosure, the cleaning solution (and process of cleaning) would be utilized at least after one resist-pattern-removal step, more specifically, Ohmi would be applied after removing a resist pattern which had been formed on top of a silicon oxide layer (note again, Ohmi's Figs. 3-6).

Returning to Wang, in Figs. 1A-1D and col. 6 (line 19) to col. 7 (line 25), a specific device manufacturing process is disclosed, and initially, it is noted that this process is very similar to the process disclosed in the current specification (see Figs. 3-8, 10, and 11 of Applicants' drawings). The point being made is that both Wang and Applicants are utilizing the common practice of:

(i) forming a pad/sacrificial oxide on a silicon wafer;

(ii) performing various processing steps including an ion implantation step "utilizing a resist mask" to form a well, wherein the resist mask is formed directly on the pad/sacrificial oxide layer;

(ii) removing the resist mask which was formed on the pad/sacrificial oxide;

(iii) removing portions of the pad/sacrificial oxide layer; and

(iv) growing a gate oxide film over the silicon wafer.

Furthermore, Note that Wang specifies another process sequence comprising:

(A) providing a silicon wafer covered with an insulating film whose main surface is mainly formed of silicon oxide (i.e., a pad oxide, note col. 4, lines 26-30; and col. 3, lines 35-36);

(B) cleaning the surface of the silicon wafer covered by said insulating film whose main surface is mainly formed of silicon dioxide after performing various steps that include ion implantation (note col. 4, lines 30-31; and col. 3, lines 49-50);

(C) removing the insulating film after step (B) thereby to expose the surface of a silicon wafer (note col. 4, line 31-33; and col. 3, lines 49-52); and

(D) after such removing, subjecting the silicon wafer to a heat treatment thereby to form a gate oxide film over the silicon wafer (note col. 4, lines 33-34; and col. 3, lines 60-62).

In regards to the instant claims, the issue of patentability rests on whether or not it would have obvious to one of ordinary skill in the art to utilize Ohmi's processing solution (and cleaning process) to clean the silicon wafer after step (iii) but before step (iv) of said common practice, ***or during step (B) of said another process sequence disclosed by Wang***. Ohmi teaches the processing solution (and cleaning process) was invented for the very purpose of removing foreign material remaining on the surface of a silicon oxide layer (i.e., a pad/sacrificial oxide surface), wherein the foreign material is a direct result of removing a resist mask which had been formed on the silicon oxide surface. Ohmi discloses in "Background Technology", cols. 1-2) prior art problems associated with foreign materials remaining after resist removal; and in col. 2 (lines 8-20), col. 3 (lines 42-47), and col. 11 (lines 29-36), Ohmi discloses the advantages of cleaning a wafer surface utilizing the processing solution. Therefore, ***it would have been obvious*** to one of ordinary skill in the art to implement Ohmi into a typical semiconductor manufacturing process (similar to that shown by Wang), wherein Ohmi's processing solution (and cleaning process) is utilized after a step of removing a resist mask which had been formed on a pad/sacrificial oxide layer ***because*** problems caused by foreign materials (from the resist mask) remaining on the pad/sacrificial oxide surface can be avoided, since Ohmi's processing solution and cleaning process will remove the foreign materials with an additional advantage of being able to perform the cleaning process at a low temperature (note Ohmi, col. 1, lines 51-65, and col. 5, lines 7-10). Lastly, utilizing an apparatus as shown by Okutani would allow Ohmi's

processing solution and cleaning process to be utilized directly after any resist removal step and before any subsequent film forming steps, wherein the apparatus will allow Ohmi to be implemented between various processing stages without exposing the substrate/wafer to a contaminating atmosphere, since the "wet process" of Ohmi can be continuously performed with various "dry processes" by using such an apparatus.

Regarding Claim 21:

Ohmi specifies the density of ammonium fluoride (i.e., hydracid fluoride salt) is in a range of 0.05 to 49 weight % (note the sentence bridging cols. 2-3), and if tetra-methyl ammonium fluoride is used for the hydracid fluoride salt, then the density is in the range of 0.05 to 60 weight %. In other words, if ammonium fluoride (NH_4F, formula weight = 37grams, i.e., 1mol of NH_4F weighs 37 grams) is used as the hydracid fluoride salt, and if the density specified by Ohmi is interpreted in grams/liter (g/L), then Ohmi could be interpreted as specifying a range 0.05 to 49 grams per liter (i.e., a range of 0.05g/L to 49g/L of NH_4F), which would convert to a range in molarity of about 0.0013 *M* to 1.324 *M* (i.e., an range of 0.0013 mol/L to 1.324 mol/L of NH_4F). It is noted that no specific hydracid fluoride salt is specified in Claim 17, therefore, the claimed range in molarity (i.e., 0.1 to 3 mol/**L**) is held obvious over the cited references because Ohmi could be interpreted as disclosing a molarity within the claimed range. In any case, Ohmi (in view of Wang and Okutani) discloses the general conditions of the instant claim, and it would have been obvious to one of ordinary skill in the art to specify a concentration of 0.1 to 3 mol/L for the hydracid fluoride salt, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding Claims 24, 29, 30:

The apparatus disclosed by Okutani allows for transporting the silicon wafer from one processing chamber (wet or dry processing) to another processing chamber without exposing the silicon wafer to (a contaminating) atmosphere. Furthermore, the apparatus includes means for completely drying the wafer after a wet process (note Okutani, col. 4, lines 29-38) and means to immediately transfer the wafer to another processing chamber after drying the wafer. Therefore, the instant claims are held obvious over the cited references.

Regarding Claim 26:

Ohmi (in view of Wang and Okutani) discloses the general conditions of the instant claim, however, Ohmi does not specify any particular range for pH. ***It is important to note Ohmi specifies that the cleaning solution is basic or at very least "shows alkalinity"(note col. 2, lines 27-39), i.e., an aqueous solution that shows alkalinity would generally be considered to have a pH greater than about 7. Although Ohmi does not specify a particular range for pH, one of ordinary skill in the art would have realized that Ohmi's disclosure is directed to a process solution having a pH of about 7 or greater, since the solution "shows alkalinity".*** It would have been obvious to one of ordinary skill in the art to specify a pH in a range of 6 to 11 for the processing solution ***because Ohmi indirectly indicates a pH range of about 7 or greater, and specifying a pH of 6 to 11 could be another way of indicating that the processing solution "shows alkalinity". In any case, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges (i.e., ranges in pH) involves only routine skill in the art. In re Aller, 105 USPQ 233***.

Regarding Claims 31 and 32:

Ohmi discloses (in col. 2, lines 35-39) the processing solution is capable of etching silicon oxide and silicon. If the main surface is mainly formed of silicon oxide, it would be clearly obvious that the processing solution etches the silicon oxide but does not etch the silicon wafer. In other words, if the main surface is a layer of silicon oxide covering the entire silicon wafer, then the processing solution would obviously etch the silicon oxide without etching the silicon wafer. To clarify, note in Ohmi's Figs. 5-6, after the cleaning step, the silicon oxide layer 4 remains, therefore, if the entire surface of the silicon wafer 3 were to be covered by the silicon oxide layer 4 such that no portion of the silicon wafer 3 were exposed, as in a case of ion-implanting through a sacrificial oxide, it would be clearly obvious to one of ordinary skill in the art that the processing solution would etch only the silicon oxide layer 4, i.e., Ohmi shows that portions of the silicon wafer 3, which are covered by the silicon oxide 4 is not etched (or will not be etched) because the cleaning step does not completely remove the silicon oxide 4 even though the silicon oxide layer 4 would be etched to some extend (as specified in col. 2, lines 35-39). The instant claims are held obvious over the cited references primarily because the limitations within these claims can be readily achieved by Ohmi's process and processing solution depending on a particular function/use of the silicon oxide layer 4, e.g., if the silicon oxide layer 4 were to be utilized as a sacrificial oxide during an ion-implantation process, as is common in the art, then no portion of silicon wafer 3 would be exposed during the "foreign material" cleaning step such that only the silicon oxide 4 will be etched during the cleaning step (note again, Figs. 5-6 of Ohmi).

4. Claim 22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmi (in view of Wang and Okutani) as applied to Claims 17 and 26 above, and further in view of Ohmi et al. (5,277,835, hereinafter, " '835 Patent").

Regarding Claims 22 and 27:

Ohmi (in view of Wang and Okutani) **lacks** a surfactant being included in the processing solution. The '835 Patent **teaches** it was well known in the art to include a surfactant into a processing solution wherein the wettability of the processing solution can be improved such that smoothness of a surface being treated can be achieved during a cleaning step (note col. 1, line 62 to col. 2, line 52). It would have been obvious to one of ordinary skill in the art to modify Ohmi (in view of Wang and Okutani) by including a surfactant because such a modification could ensure smoothness of a surface being cleaned by the processing solution.

5. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmi (in view of Wang and Okutani) as applied to Claim 17 above, and further in view of Wolf ("Silicon Processing for the VLSI Era: Volume I", 1986).

Regarding Claim 28:

Ohmi (in view of Wang and Okutani) disclose the general conditions of the instant claim except for specifying parameters for growing the gate oxide film. Wolf is cited only to show that it was very well known in the art that thermal oxide can be grown by a heat treatment preformed in a mixed atmosphere of water and oxygen at a temperature in a range of 800° to 900 °C (see underlined text in pages 198 and 201). The instant claim is held obvious over the cited

references primarily because the claimed parameters are typically used when forming a thermal oxide layer.

Remarks

6. Applicant's remarks/arguments have been carefully reviewed and considered; however, they are not persuasive for the following reasons.

In response to Applicant's arguments regarding the combinations of references, it is initially noted Ohmi et al. (5,990,060, hereinafter, Ohmi) disclose the processing solution will effectively clean debris located directly on an insulating film or directly located on a silicon wafer, i.e., the processing solution will effectively clean a main surface of a substrate wherein the main surface is an insulating film or a silicon wafer (note especially, Ohmi's Fig. 5 and Fig. 7, wherein debris "6" is located on either insulating film "4" or on silicon wafer "3"). Applicant submits that Ohmi is primarily concerned with performing a cleaning step after formation of a gate oxide and gate electrode (see page 9, lines 1-3); however, it is clear from at least the embodiment shown in Figs. 7-10 that Ohmi discloses the processing solution can be used in a cleaning step before any layers are formed (e.g., a gate oxide layer). Therefore, Applicant's remarks regarding Ohmi's disclosure is not persuasive. Applicant submits that Ohmi lacks performing a cleaning process prior to forming a gate oxide, i.e., Applicant emphasizes the criticality of performing the cleaning step using the recited (claimed) processing solution, at the recited process in the sequence of steps as recited in the present claims (see Applicant's remarks in the last two paragraphs on page 9). On pages 6-7 of this Office action (note text that is underlined, italicized, and bold-typed), Wang has been cited to show that is was common in the

art to perform a cleaning step prior to formation of a gate oxide, wherein the cleaning is applied to an insulating layer (i.e., a pad oxide) covering a silicon wafer. The criticality of performing a cleaning step prior to formation of a gate oxide is disclosed by Wang; and given Ohmi's disclosure, one of ordinary skill in the art would have realized that Ohmi's processing solution would be an ideal cleaning solution to use during the cleaning steps specified by Wang, since Wang performs the cleaning step to remove debris that apparently results form prior processing steps that would include, for example, ion implantation, resist removal, etc. Applicant's submission of the publication Cleaning Technology For Silicon Wafer Surface (February 28, 1995) has been noted. Applicant submits that, in the involved art, different cleaning solutions are used prior to, and subsequent to, forming a gate oxide film (page 11, last paragraph). It is important to note that Ohmi does not limit the processing solution to a cleaning process that is performed only before (or only after) forming a gate oxide film (note the location of debris in Figs. 5 and 9), in other words, one of ordinary skill in the art would have realized that Ohmi's processing solution can be used to clean a gate oxide film **or** to clean a surface prior to forming a gate oxide film, or for that matter, nothing in Ohmi's disclosure restricts one from using the processing solution to clean ***before*** forming a gate oxide film **and** ***after*** forming a gate oxide film. Applicant's remarks with respect to said publication are not persuasive primarily because the cleaning process outlined in the publication would not be the only way to clean a substrate during device fabrication. In summary, all pending claims are held obvious primarily because Ohmi discloses a critical aspect of the current invention (i.e., the processing solution), and given Wang's disclosure, one of ordinary skill in the art would have realized that Ohmi's processing

solution would be an ideal cleaning solution to utilize during the cleaning steps specified by Wang.

Status of the Claims

7. Claims 17-32 are pending.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 703-306-5986.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Lex Malsawma

May 28, 2003

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800